AMENDMENTS TO THE CLAIMS

1. (Original) A jitter inducing circuit comprising:

a plurality of delay means for delaying rising and/or falling edges of pulses of a reference pulse train,

a signal composer for composing the outputs of a plurality of said delay means,

a delay time setup means for setting the delay times of said rising and/or falling edges to a plurality of said delay means,

a switch means for selectively providing the pulses of said reference pulse train to one of a plurality of said delay means, and

a switch control means for controlling said switch means to provide said pulses to one delay means in which the setup of said delay time has finished.

2. (Original) A jitter inducing circuit recited in claim 1 further comprising:

an input delay means for delaying said reference pulse train so that said switch control means receives said reference pulse train before said switch means to control said switch means according to the input of the reference pulse train.

3. (Original) A jitter inducing circuit recited in claim 1 wherein said delay time setup means changes said delay time as a function of a delay time transition waveform.

4. (Original) A jitter inducing circuit recited in claim 1 wherein said delay means has a buffer circuit for providing non-inverted and inverted outputs, a first delay circuit for delaying said non-inverted output by a preset delay time, a first one-shot pulse circuit for converting the output of said first delay circuit into one-shot pulse, a second delay circuit for delaying said inverted output by a preset delay time, a second one-shot pulse circuit for converting the output of said second delay circuit into one-shot pulse, and a logic circuit for providing a logic signal according to the outputs of said first and second one-shot pulse circuits.

5-7. (Cancelled)

8. (Previously cancelled)

9. (Original) A jitter inducing method comprising the steps of:

setting delay times of rising and/or falling edges of pulses in a reference pulse train in a first delay block selected from a plurality of delay blocks,

delaying said reference pulse train by said first delay block and providing an output to an output terminal,

setting delay times of the rising and/or falling edges of pulses in a reference pulse train to a second delay block selected from a plurality of delay blocks other than said first delay block,

switching the supply of the reference pulse train to said second delay block from said first delay block, and

delaying said reference pulse train by said second delay block and providing an output to said output terminal.

10. (Original) A jitter inducing method recited in claim 9 wherein said delay times to the plurality of said delay blocks are controlled as a function of time so that the change of said delay time traces a desired function.

11. (Original) A circuit for generating a pulse train comprising:

a plurality of delay blocks for delaying rising or falling edge of a provided pulse according to a preset delay time,

a pulse providing means for providing a pulse to be jittered and a pulse not to be jittered to separate delay blocks of the plurality of said delay blocks wherein both said pulses are derived from a reference pulse train,

a signal composing means for composing the outputs of the plurality of said delay blocks, and

delay time setup means for setting said delay times for the rising or falling edges of said pulses to the plurality of said delay blocks,

wherein said delay times for said delay block to which said non-jittered pulse is provided is fixed, and said delay time of said delay block to which said pulse to be jittered is provided changes sequentially.

12. (Original) A pulse generating method comprising the steps of:

a) generating a pulse to be jittered and a pulse not to be jittered based on a reference pulse train,

b) delaying the rising edge or the falling edge of said pulse to be jittered according to a preset delay time,

c) composing said non-jittered pulse and said pulse delayed in step (b), and

d) repeating steps (a) through (c) wherein said delay time in said step (b) changes every time.